Modeling and Design Aspects of Millimeter-Wave Schottky Varactor Frequency Multipliers

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***Abstract*— Design and optimization of frequency multipliers for millimeter and submillimeter wavelengths have been previously performed using harmonic-balance techniques together with equivalent circuit models. Using this approach it is difficult to simultaneously design and optimize the diode device and the multiplier circuit. This work demonstrates results from numerical semiconductor simulation coupled with the harmonic-balance technique. The good agreement between the calculated and published experimental data for the output power and efficiency is essentially due to the incorporation of impact ionization in the numerical model. Details on the device behavior and circuit operation at different power levels are provided.**

***Index Terms*— Frequency multipliers, nonlinear circuit analysis, numerical modeling, Schottky diode modeling, semiconductor simulation, submillimeter-wave multipliers.**

I. Introduction

VARACTOR frequency multipliers play a vital role in developing all-solid-state power sources at terahertz frequencies. The modeling and design of Schottky varactor frequency multipliers have received considerable attention due to the progress in device and circuit performance. The key points in this progress have been the enhanced physical understanding of Schottky diode varactor operation [1] and the improvement in analysis methods [2], [3], Schottky diode models [3]–[5], as well as numerical physical device models [2], [6], [7]. In the present work we focus on frequency multiplier analysis based on coupling the circuit-oriented harmonic-balance analysis with drift-diffusion numerical semiconductor device simulation. Such an approach enables to concurrently optimize the device electrical and geometrical parameters together with achievable output power, conversion efficiency, and the required loads at the specific harmonics. Our simulator incorporates accurate boundary conditions for high forward as well as reverse bias, including impact-ionization, series resistance effects, and self-consistent implementation of image-force lowering and tunneling effects [6]–[8].

II. Determining Factors for Mulitplier Performance

Many of the previously observed discrepancies between measured and calculated results are not directly related to the complexity of Schottky diode model but can have a simple explanation due to multiplier circuit operation. At low input power levels the performance of the multiplier is mainly determined by the dc bias point and the load impedances at the fundamental and output frequencies, whereas at high power levels the operation is affected by the breakdown properties of the employed device and its series resistance. The highest conversion efficiency of frequency multipliers is obtained in the transition region between low- and high-power regime and can be only obtained for inductive loads at higher harmonics. The discussion presented below is based on experimental and calculated results for different varactor diodes and different multiplier circuits published in [2], [3], and [8] together with original calculations utilizing our model presented here.

The diode structure has been discretized with a nonuniform mesh utilizing the structure data given in the publications. The simulation domain includes the epitaxial and substrate layers. The total current waveform at the terminals of the device, consisting of a sum of the conduction and the displacement currents, is used in the harmonic-balance program. The harmonic-balance program solves the circuit equations by optimization techniques [6].

A. Low-Input Power Levels

At low power levels the amplitude of the voltage waveform is smaller than the absolute value of the bias voltage and electron saturation effects are not significant. Therefore, it is possible to maximize the output power and the efficiency of the frequency multiplier by choosing an appropriate bias point and optimum loads at the different harmonics. Most simulators overestimate the multiplier output power and the efficiency at low power levels. This can be inferred from Fig. 1, where the output power and the efficiency have been plotted versus the input power for a frequency doubler utilizing an UVA 6P4 Schottky varactor. The results have been taken from [2] with additional simulations from our model. All simulators overestimate the output power [Fig. 1(a)] and the efficiency [Fig. 1(b)] of the doubler at power levels $P_{\rm in} \leq 10$ dBm. None of the simulators in [2] [indicated as Monte Carlo coupled with harmonic-balance (MCHB), drift-diffusion with field-dependent mobility (DDHB-fdm), and drift-diffusion with averaged constant mobility (DDHB-am) in Fig. 1] is able to predict the correct power slope and the MCHB code [2] performs worst. Results from our model agree well with measurements for input powers above $P_{\rm in} \geq 11$ dBm and reproduce the measured slope. The diode parameters have been taken from [2], the bias voltage was set to $V_{\rm bias} =$

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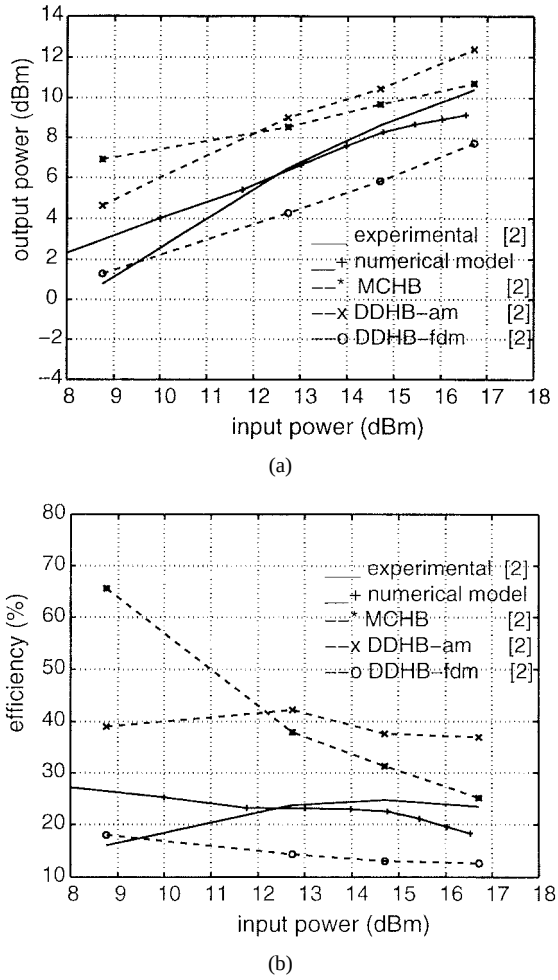

Fig. 1. Calculated and measured (a) output power and (b) conversion efficiency as a function of the input power for a UVA 6P4 frequency doubler. The fundamental frequency is $f_0 = 100$ GHz. The solid line with symbols "+" illustrates the results from our model, the solid line shows the experimental results from [2], and the dashed lines represent calculated results from [2].

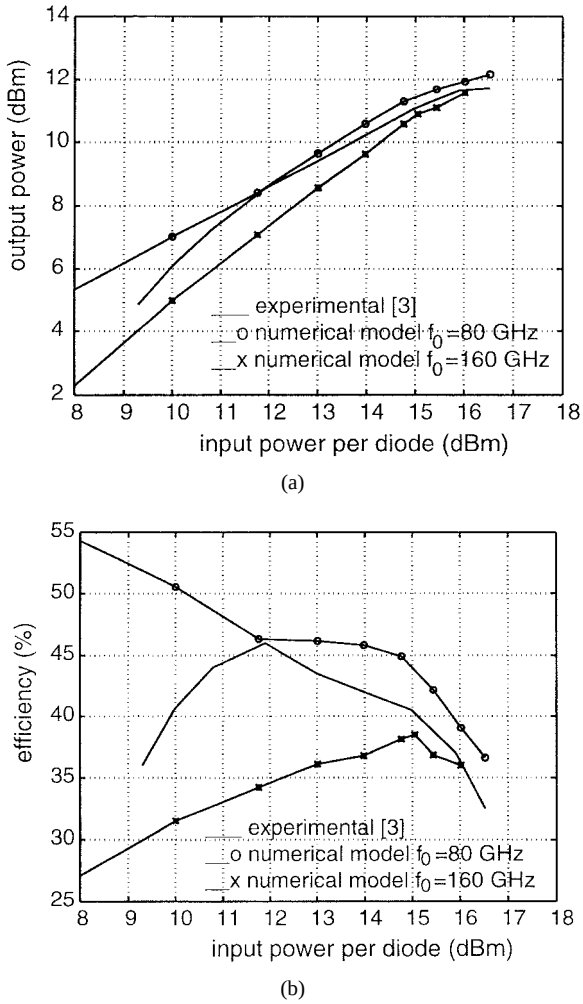

Fig. 2. Calculated and measured [3] (solid line) (a) output power and (b) conversion efficiency as a function of the input power for a frequency doubler. Calculated results are illustrated as symbols "o" for $f_0 = 80$ GHz and as circles "+" for $f_0 = 160$ GHz, respectively.

$-10\,V$ and the loads at harmonic frequencies were set to $Z(nf_0) = (0 + j0)\,\Omega$ for $n > 2$. The load impedance at the output $Z(2f_0)$ was optimized for maximum output power for each input power [approximately $Z(2f_0) = (70 + j200)\,\Omega$ at $P_{\text{in}} = 14$ dBm], while the diode was matched at the fundamental frequency. The matching of the diode at each power level at the fundamental and output frequency is responsible for the unrealistic results from the simulations, because the diode matching is generally optimized for high power levels in experimental systems. Matching of the diode at low input powers is sensitive to changes with power, frequency, and bias voltage due to the high quality factor $Q = \Im\{Z(f_0)\}/\Re\{Z(f_0)\} \approx 10 \cdots 20$. Hence, we believe that any simulation program capable of accurately simulating the device junction capacitance and series resistance could be used for this operating regime.

The situation is emphasized in Fig. 1(b) which shows that the results from the Monte Carlo code predict an efficiency close to the theoretical limit at low input power levels, whereas the measured efficiency is low and increases with increasing drive level. In our simulations we have used the geometrical area of the device and it is outlined in Section II-C that the agreement between our results and measurements could be still improved by taking the effective diode area in the simulations.

B. High Input Power Levels

Based on the results in [1] many publications have dealt with current saturation mechanism in frequency multipliers, disregarding the effect of impact ionization. Our simulations include impact ionization effects and demonstrate that a substantial dc current flows at increased power levels. For frequency multipliers at fundamental frequencies $f_0 \approx 100$ GHz electron scattering effects can be neglected and the important parameters affecting multiplier performance are the current dependent series resistance and impact ionization. The efficiency in Fig. 1 decreases with the onset of increased current flow due to impact ionization, although the output power is still increasing. The effect of the variation of the load impedances is weak ($Q \approx 4$) because the voltage excursion is over the full reverse characteristic of the diode. Our simulations also show a strong increase of $\Re\{Z(f_0)\}$ in accordance with [1] and [3]. We have also compared our simulations with the measured data for a frequency multiplier using a similar diode at $f_0 = 80$ GHz [3] illustrated in Fig. 2. At the

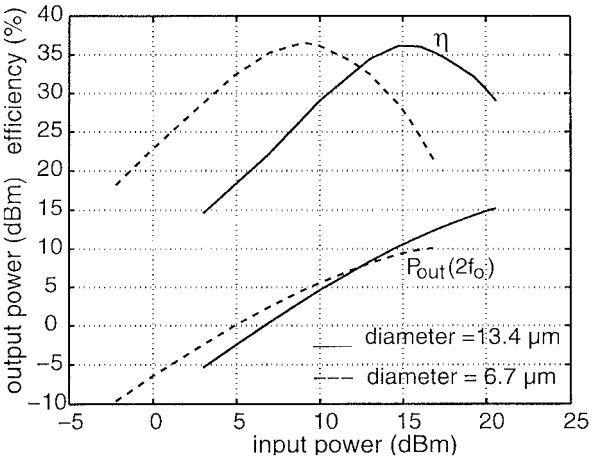

Fig. 3. Calculated output power $P_{\rm out}$ and conversion efficiency η as a function of the input power for two Schottky varactor diodes D734 from the TU Darmstadt. The fundamental frequency is $f_0 = 50$ GHz.

output the balanced diode configuration has been simulated as a direct parallel connection of two identical diodes. The agreement with measured data is very good. Simulations of the same arrangement at $f_0 = 160$ GHz also agree well at high input power levels, while we cannot reproduce the measured efficiency at low and intermediate power levels. Although the simulation presented in Figs. 1 and 2 have been performed at different frequencies and with different circuit structures, we achieve very good agreement at large power levels, which demonstrates that at high power levels the diode device performance is more important than the embedding circuit.

C. Optimization of Conversion Efficiency

At low frequencies frequency multipliers should be optimized for maximum output power, because sufficient power is available for pumping the diode. At increased frequencies it is desirable to improve the conversion efficiency, which requires the optimization of both the multiplier circuit and the varactor diode device.

An analysis of the loads presented to the diode suggests that the optimum termination should be inductive with an improvement of up to 20% in efficiency for large inductive loads at $3f_0$. It is insensitive to the bias and input power level even if the inductance is slightly lossy. A capacitive load at $3f_0$ can provide an improvement in efficiency of up to $\approx$5%. The maximum conversion efficiency can be shifted with regard to the input power by choosing Schottky diodes with different areas. Fig. 3 illustrates calculated results for Schottky varactor diodes D734 from the TU Darmstadt [6]. Although these diodes have been designed for higher operating frequencies, the results presented in Fig. 3 are at $f_0 = 50$ GHz in order to shorten the simulation time. The maximum conversion efficiency is shifted toward lower values of the input power when the diode area is decreased. This is because impact ionization is also a function of the current density in the device. The important result here is that the demand for maximum conversion efficiency at a prescribed input or output power uniquely determines the diode area.

III. Conclusions

We have demonstrated that at low input power levels the operation of the multiplier is mainly determined by the embedding circuit and the diode dc operating point. The discrepancies between the measured and the calculated results observed in many simulations could be explained by mismatching effects in the circuit, while effects due to device physics seem to be insignificant. In contrast at high power levels the contribution of the embedding circuit to the overall performance of the multiplier is marginal and impact ionization in the device is responsible for output power saturation and conversion efficiency decrease. We have obtained good agreement between published experimental results and our calculations for frequencies up to 200 GHz with our enhanced drift-diffusion model coupled to a harmonic-balance simulator.

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